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EXAMINER	
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ART UNIT	**PAPER NUMBER**
2665	15

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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/293,563	BIANCHINI, RONALD P.	
	Examiner	Art Unit	
	Steven HD Nguyen	2665	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *08 October 2003*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-5 and 7-25* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-5 and 7-25* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. §§ 119 and 120

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

13)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application) since a specific reference was included in the first sentence of the specification or in an Application Data Sheet. 37 CFR 1.78.

a) ☐ The translation of the foreign language provisional application has been received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121 since a specific reference was included in the first sentence of the specification or in an Application Data Sheet. 37 CFR 1.78.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 1-5, 15-16 and 18-21 are rejected under 35 U.S.C. 103(a) as being unpatentable over Haddock (USP 6034957) in view of Nelson (USP 6061358).

Regarding claims 1, 3-5, Haddock discloses (Fig 1-5 and col. 1, lines 15 to col. 40) a switch system (Fig 1, 100) comprising at least one input port mechanisms (Fig 1, MAC 1) for receiving the packets; at least one output port mechanisms (Fig 1, MAC 1) for transmitting the packets; a carrier mechanism (Fig 1, the bus between data path control 120 and packet memory 130) which connects to each input port mechanism and each output port mechanism for conveying the packets in an allocated time slot ; a memory mechanism (Fig 1, Ref 130) which connects to the carrier mechanism, stores the packets and a mechanism for providing data from more than one packet at a time to the memory mechanism through the carrier mechanism from the input port mechanisms (Fig 1, Ref 160), said providing mechanism transferring more than one packet at a time in the allocated time slot whose total width equals the width of the carrier mechanism in each allocated time slot to the memory mechanism (the data control path provides the received data packets from the input port to the memory 130) and a width of carrier mechanism is wider than the width of input and output port mechanism (Fig 2, the input bus has a wide 16 which is less than the bus coupled to the memory 256, 512, 1024 etc) so the data from

more than one packet at a time is transferred in the allocated time slot and the providing mechanism transferring more than one packet at a time to the memory in the allocated time slot only when there is enough data from more than one packet from an input port to fill the width of carrier mechanism but not transferring any data from any packets from the input in the allocated time slot when there is not enough data to fill the width of the carrier (col. 6, lines 54-66, the data only transfers when it accumulates enough data to fill the bus 121) and the providing mechanism including input stage queue groups for storing the received data from input port and output state queue groups for storing the data for transmitting to output port (Fig 2a, Ref 220 is an input stage buffer groups and Fig 2b, Ref 260 is output stage buffer groups for transmitting the data onto the output port) and transmitting/receiving a variable sized packets (See col. 5, lines 42-62) and the providing mechanism also provides packets from the memory mechanism to the output port mechanisms through the carrier mechanism, said providing mechanism transferring packets or portions of packets whose total data equals the width of the carrier mechanism in each transfer cycle from the memory mechanism (Fig 2 for transferring the data packets between the input 210 and output 260 via memory 130). However, Haddock fails to disclose the carrier mechanism for carrying packets in an allocated time slot. In the same field of endeavor, Nelson discloses a method for transmitting the packets via an allocated time slot of the carrier mechanism (col. 2, lines 9-40).

Therefore, it would have been obvious to one of ordinary skill in the art for apply a method of transmitting the data packets via an allocated time slot in TDM bus as disclosed by Nelson's system into Haddock's switch. The motivation would have been to improve a throughput of the switch.

Regarding claim 2, Haddock implicitly discloses the width of the carrier mechanism is independent of the width of any packet (the bus only need to fill the bus width based on the received data).

Regarding claim 15, Haddock discloses (Fig 1-5 and col. 1, lines 15 to col. 40) a switch comprising a central resource (Fig 1, Ref 120 has a width and bandwidth and input and output port) having a width and an overall bandwidth and input port mechanisms and output port mechanisms each having widths for receiving or sending packets, respectively, said central resource width independent of any input or output port mechanisms width and the overall bandwidth can grow without limitation by input or output port mechanism width (See col. 5, lines 43 to col. 6, lines 5); and a memory mechanism for storing packets, said memory mechanism connected to the central resource (Fig1, Ref 130) and receiving more than one packet at a time is a respective time slot from the central resource which completely fills the width of the central resource; the central resource transferring more than one packet at a time to the memory in the respective time slot only when there is enough data from more than one packet to fill the total width but not transferring any data from any packets in the respective time slot when there is not enough data to fill the total width of the carrier (col. 6, lines 54-66, the data only transfers when it accumulates enough data to fill the bus 121). However, Haddock fails to disclose said central resource partitioned via time slots that are allocated to the input and output port mechanisms. However, in the same field of endeavor, Nelson discloses a central resource for dividing to the time slot for allocating to the input port and output port (See col. 2, lines 9-66).

Therefore, it would have been obvious to one of ordinary skill in the art for apply a method of dividing the central resource into the time slots as disclosed by Nelson's system into Haddock's switch. The motivation would have been to improve a throughput of the switch.

Regarding claim 16, Haddock discloses the central resource includes a memory bus (Fig 1, Ref 130).

Regarding claim 18, Haddock discloses (Fig 1-5 and col. 1, lines 15 to col. 40) a switch comprising a time division multiplex bus having a width (Fig 2A, Ref 121); a memory mechanism connected to the bus which is accessed via time slots of time division multiplexing of the bus (Fig 2A, Ref 130); and a mechanism for reading and writing data of packets to the memory mechanism through the bus without knowledge of the packet boundaries of the data and the reading and writing mechanism in a respective time slot only when there is enough data from more than one packet to fill the width but not transferring any data from any packets in the respective time slots when there is not enough data to fill the width of the bus (col. 6, lines 54-66, the data only transfers when it accumulates enough data to fill the bus 121). However, Haddock does not fully disclose the bus is a TDM bus having a plurality of time slots. In the same field of endeavor, Nelson discloses a TDM bus having a plurality of time slot for carrying the data packets (See col. 2, lines 9-66).

Therefore, it would have been obvious to one of ordinary skill in the art for apply a TDM bus having a plurality of time slots as disclosed Nelson's system into Haddock's switch because Haddock suggests a selector for selecting the data from one of plurality of inputs onto the memory bus. The motivation would have been to improve a throughput of the switch.

Regarding claim 19, Haddock discloses (Fig 1-5 and col. 1, lines 15 to col. 40) a switch comprising a time division multiplex carrier mechanism having a width (Fig 2A, ref 121); a memory mechanism (Fig 2A, Ref 130) connected to the carrier mechanism; and an input stage mechanism having a width for providing data of packets to the memory mechanism so the data of the packets fills the width of the bus via time division multiplexing, said bus width a positive non-integer multiple of the input stage mechanism width; a mechanism for providing data of packets having a width to the memory so the data of packets fills the width of the bus via TDM, said bus width being a positive non integer multiple of the packet width greater than one; the input stage mechanism transferring more than one packet at a time to the memory mechanism in a respective time slot only when there if enough data from more than one packet to fill the width but not transferring any data from any packets in the respective time slot when there is not enough data to fill the width of the carrier (col. 6, lines 54-66, the data only transfers when it accumulates enough data to fill the bus 121; See Fig 2). However, Haddock fails to disclose a carrier mechanism is TDM having a plurality of time slot. In the same field of endeavor, Nelson discloses a TDM bus having a plurality of time slot for carrying the data packets (See col. 2, lines 9-66).

Therefore, it would have been obvious to one of ordinary skill in the art for apply a TDM bus having a plurality of time slots as disclosed Nelson's system into Haddock's switch because Haddock suggests a selector for selecting the data from one of plurality of inputs onto the memory bus. The motivation would have been to improve a throughput of the switch.

Regarding claims 20-21, Haddock discloses (Fig 1-5 and col. 1, lines 15 to col. 40) a switching packets comprising receiving a first packet and at least a second packet at a switch

mechanism (Fig 1); and transferring data of the first packet and the second packet to a memory mechanism (Fig1, ref 130) via time slots time division multiplexing (Fig 2, Ref 10) of a bus having a width, said bus width not a function of the data contained in any packet and transferring the data only when data from the packets fills a predetermined portion of the width of the bus in a time slot, but not transferring any data from the first and second packets in the time slot when there is not enough data to fill the predetermined portion of the width of the bus (col. 6, lines 54-66, the data only transfers when it accumulates enough data to fill the bus 121). However, Haddock fails to disclose a carrier mechanism is TDM having a plurality of time slot. In the same field of endeavor, Nelson discloses a TDM bus having a plurality of time slot for carrying the data packets, which has a width, is 256 bytes (See col. 2, lines 9-66 and Table 1).

Therefore, it would have been obvious to one of ordinary skill in the art for apply a TDM bus having a plurality of time slots as disclosed Nelson's system into Haddock's switch because Haddock suggests a selector for selecting the data from one of plurality of inputs onto the memory bus. The motivation would have been to improve a throughput of the switch.

3. Claims 7-14, 17 and 22-25 are rejected under 35 U.S.C. 103(a) as being unpatentable over Haddock and Nelson as applied to claims 1, 15 and 20 above, and further in view of Fukano (USP 5774453).

Regarding claims 7-9, Haddock and Nelson do not disclose the claimed invention. However, Fukano discloses (Fig 1-2 and col. 1, lines 6 to col. 7, lines 63) the providing mechanism includes a classifying mechanism which places a packet which is received by the input port mechanism into a corresponding queue group, said classifying mechanism connected to the input port mechanisms and the input stage queue groups (Fig 1, Ref 11 discloses a

classified mechanism for classifying the packets into a queue group); a processing mechanism which places a packet in an output stage queue group into a corresponding output port mechanism, said processing mechanism connected to the output port mechanisms and the output stage queue groups (Fig 1, ATM switch has a processing means for placing the packets into a corresponding of output queue); the classifying mechanism (Fig 1, Ref 11 has a classifier for inputting a packet in a corresponding queue) includes a first write finite state machine for writing packets into a corresponding input stage queue, the providing mechanism includes a second write finite state machine for writing packets from an input stage queue group into the memory mechanism (Fig 1, ref 13 discloses the packets in the input queue are transferred to the shared memory) , and a first read finite state machine for reading packets from the memory mechanism to an output stage queue group, and the processing mechanism includes a second read finite state machine for reading a packet from the output stage queue group to the network (Fig 1, ref 18 has a read port for reading the packets in the shared memory into the corresponding queues of the output port) and the first read finite state machine only transfers data of packets of an input stage queue group to the bus when the input queue group contains at least one cache-line of data (See Fig 1, the input buffer will transmit the packet to the bus when it has a data).

Therefore, it would have been obvious to one of ordinary skill in the art for apply a buffer into an input port for storing the packet before transferring into a shared memory of the switch as disclosed Fukano's switch into the switch of Haddock and Nelson. The motivation would have been to improve a throughput of the switch.

Regarding claim 10, Haddock discloses the memory mechanism includes a shared memory (Fig 1, ref 130).

Regarding claim 11, Haddock discloses packets or portions of packets travel on the carrier mechanism (Fig 2a, Ref 121).

Regarding claim 12, Haddock discloses the carrier mechanism includes a bus (Fig 2a, Ref 121).

Regarding claims 14 and 25, Haddock discloses the communication line is an ATM network (col. 1, lines 45-65) and memory stored the packets without knowledge of the packet boundaries of the packet (See Fig 2, the packets are stored in the memory without knowledge of the boundaries of the packet.

Regarding claim 17, Haddock fails disclose the claimed invention. However, Fukano discloses (Fig 1-2 and col. 1, lines 6 to col. 7, lines 63) the central resource includes queue groups in which packets are classified, and the packets are read from and written into the memory mechanism from the queue groups (Fig 2).

Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention was made to apply an input buffer for storing the classified packet into the queue group as disclosed by Fukano into the switch of Haddock and Nelson. The motivation would have been to reduce the latency of higher priority packet and prevent a dead lock in the switch.

Regarding claims 13 and 22-24, Haddock discloses before the transferring data step there is the step of determining that the input-stage queue group has at least enough data to fill the predetermined portion of the width of the bus before data is transferred to the bus and before the transferring data step, there is the step of determining that the input stage queue group has at least one-cache line of data (col. 6, lines 54-66, the data only transfers when it accumulates enough data to fill the bus 121). However, Haddock and Nelson fails to disclose the first and

second packets stored in the queue. In the same field of endeavor, Fukano discloses (Fig 1-2 and col. 1, lines 6 to col. 7, lines 63) the steps of placing the first packet and at least the second packet in an input stage queue group (Fig 1, Ref 11).

Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention was made to apply an input buffer for storing the classified packet into the queue group as disclosed by Fukano into the switch of Haddock and Nelson. The motivation would have been to reduce the latency of higher priority packet and prevent a dead lock in the switch.

Response to Arguments

4. Applicant's arguments filed 10/8/2003 have been fully considered but they are not persuasive.

In response to pages 12, the applicant states that Haddock and Nelson do not discloses a carrier mechanism having a width wider than the width of input and output port mechanisms so data from more than one packet at time is transferred in the allocated time slots; providing mechanism transferring more than one packet at a time in the allocated time slots whose total width equals the width of the carrier mechanism or only when there is enough data from more than one packet from input stage queue group fill the width bus not transferring any data from any packets from the input stage queue groups in the allocated timeslot when there is not enough to fill the width of the carrier mechanism. In reply, Haddock discloses a carrier mechanism for transferring packets, which receive, from input port having a width less than width of bus between the input port and memory, to memory. Therefore, the bus for carrying the data packets from input port to memory via the sub paths "allocated time slots" wherein each sub path can be

carried from 64 bits of the packet. These sub paths can carry more than one packet from the input port to the memory when the packets have 65 "520 bit" byte packet and each sub path has a wide 64 bit. So 16-sub path will carry 1024 bit data, which is more than one packet in the allocated sub paths "time slot". Furthermore, Haddock discloses the providing mechanism will read the data from the input port onto the carrier mechanism more than one packet at a time in the allocated time slots whose total width equals the width of the carrier mechanism or only when there is enough data from more than one packet from input stage queue group fill the width bus not transferring any data from any packets from the input stage queue groups in the allocated timeslot when there is not enough to fill the width of the carrier mechanism such when the packets have 65 "520 bit" byte packet and each sub path has a wide 64 bit. So 16 sub path will carry 1024 bit data which is more than one packet in the allocated sub paths "time slot" and Nelson discloses a bus with which uses for reading the data packet from input port into memory is 256 bytes which is greater than more than one short data packet "65 bytes"; see table 1 as set forth in the paragraph 2 of the final office action of claim 1.

Conclusion

5. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period

will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Steven HD Nguyen whose telephone number is (703) 308-8848. The examiner can normally be reached on 8-5.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Huy D Vu can be reached on (703) 308-6602. The fax phone number for the organization where this application or proceeding is assigned is (703) 872-9314.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 305-4700.

Steven HD Nguyen
Primary Examiner
Art Unit 2665
12/22/2003